Ultra-low-power computing

Keywords : Microcontroller; Memory; Flip-flops; Adaptive circuits; 28 nm CMOS; IoT.

David Bol, François Stas, Thomas Haine, Ludovic Moreau, Guerric de Streel, Charlotte Frenkel, Khoi Nguyen, Denis Flandre, Jean-Didier Legat

Abstract – For a massive yet sustainable Internet-of-Things, ultra-low-power computing is required without compromising the data processing and storage performances. In the electronic circuits and systems (ECS) group, we pursue new solutions to this challenge with ultra-low-voltage (ULV) digital integrated circuit (IC) and system-on-chip (SoC) design. Latest results feature the evaluation of 28 nm FDSOI CMOS technology for ULV digital circuits and SRAM memories, adaptive back biasing techniques to compensate process and temperature variations and low-energy pulsed flip-flops in collaboration with CEA-LETI.

The connection of our daily life's objects to the cloud according to the Internet-of-Things (IoT) vision is about to revolutionize the way we live. To enable this revolution, a massive deployment of sensor nodes is required with predictions announcing up to trillions of these nodes. Such a massive deployment is not environmentally and economically sustainable with current technologies. Some of the pitfalls lay in the computing capability of IoT nodes whose power consumption needs to be optimized in order to operate on ambient energy harvesting without compromising the data processing and storage performances [1]. Indeed, key applications using audio/vision sensing or brain-machine interfaces (Fig. 1) require the on-chip extraction of the important information from the sensed data to limit the worldwide electrical power consumption of the ICT infrastructure (datacenters and basestations) due to machine-to-machine (M2M) wireless data traffic. Therefore, the IoT nodes need to be able to perform compression, feature extraction or classification within their ultra-low power budget which is not possible with current low-power microcontroller (MCU) technologies because of their limited energy efficiency.

The energy cost of software execution can be avoided by adding key dedicated hardware accelerators to the MCU [2]. ULV operation can further improve the energy efficiency of the HW accelerators. Nevertheless, ULV operation comes at the expense of a degraded speed ultimately below the MHz deep in the subthreshold regime. To overcome the performance degradation, we rely on nanometer CMOS technologies [1] with high-speed design techniques for both logic and memories in 28 nm FDSOI CMOS including:

- the optimization of SRAM memories with respect to their dynamic and statistical stability [3],
- the generation of adaptive back biasing voltages to compensate process and temperature effects on the speed of logic and SRAM memories [4],
- the design of ultra-dense low-clock load pulsed flip-flops in collaboration with CEA-Leti (Grenoble, France) [5] and true-single-phase flip-flops.

Some of these techniques have been used to design a 0.4V ultra-low-power SRAM memory whose prototype codenamed MEMPHIS is under test (Fig. 2). Its dual-voltage divided-wordline architecture featuring the UCL patented ULP SRAM bitcell with adaptive back biasing and low-energy skewed sense amplifiers should allow 100-MHz operation with record access energy. Next research will focus on the design of a high-performance ULV MCU-based computing platform in 28 nm FDSOI CMOS.

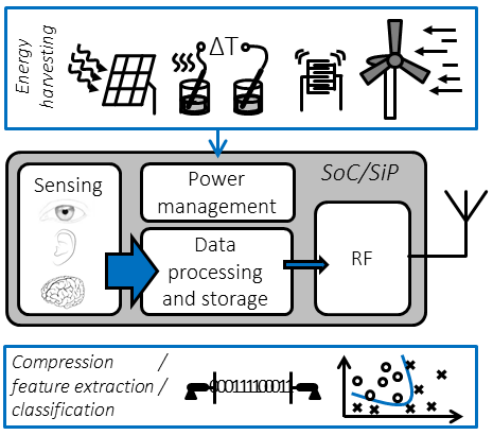

Figure 1: Data processing and storage in IoT nodes need to perform compression, feature extraction of classification at an ultra-low power.

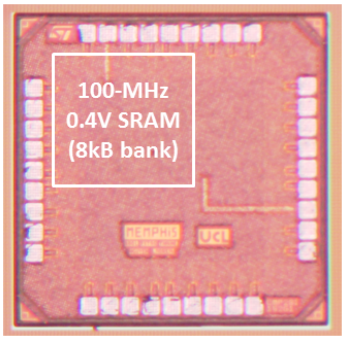

Figure 2: Die microphotograph of the MEMPHIS prototype in 28 nm FDSOI CMOS.

References

[1] D. Bol, G. de Streel and D. Flandre, "Can We Connect Trillions of IoT Sensors in a Sustainable Way? A Technology/Circuit Perspective," in IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 49-50, 2015.

[2] L. Moreau, "Conception d'une Plateforme SoC de Traitement de Signaux Numériques à Ultra-Basse Consommation pour la Détection des Crises d'Epilepsie", Master Thesis, UCL, 2014.

[3] A. Elthakeb, T. Haine, D. Flandre, Y. Ismail, H. Abd Elhamid and D. Bol, "Analysis and Optimization for Dynamic Read Stability in 28 nm SRAM Bitcells", in Proc. IEEE Int Conf. Circuits and Systems, pp. 1414-1417, 2015.

[4] Q.-K. Nguyen, "Adaptive Back Biasing System for Compensation of PVT Effects on SRAM Dynamic Stability", Master Thesis, UCL, 2015.

[5] S. Bernard, M. Belleville, A. Valentian, J.-D. Legat and D. Bol, "Experimental Analysis of Flip-Flops Minimum Operating Voltage in 28 nm FDSOI and the Impact of Back Bias and Temperature", in Proc. International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), 2014.