Wide frequency band assessment of advanced MOSFET architectures in a view of analog and RF applications

Keywords : Advanced MOSFET; UTBB FDSOI; FinFET; NanoWire; Analog/RF Performance.

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Enormous progress of the semiconductor technology during the last decades was driven by the continuous demand for the increase of the operation speed and the integration density of complex digital circuits. Aggressive device downscaling requests for employment of new materials and non-classical device architectures.

Nowadays, two main contenders are recognized as pretenders to satisfy ITRS requirements for the 20 nm device node and beyond:

- planar fully depleted (FD) Silicon-on-Insulator (SOI) with ultra-thin body and ultra-thin buried oxide (BOX): UTBB MOSFET;
- multiple-gate (MuG) MOSFET (FinFET and NanoWire FET).

Last years our team was involved in EU projects on the development of cutting-edge MOSFET technology with industrial and RI leaders in the domain, such as ST-Microelectronics (Fr), CEA-Leti (Fr), IMEC (Be). Thanks to this collaboration, EC and FNRS fundings, we had possibility to assess various advanced MOSFETs in the view of their further analog/RF applications [1]. Both UTBB and MuG architectures were revealed to be promising for mobile/wireless applications with LOP/LSTP options with a potential for improvements [1].

Device analog/RF performance was assessed through key figures such as transconductance (g_m), output conductance (g_d), intrinsic gain (A_{vo}), cut-off frequencies (f_T, f_{max}). Particular attention was paid to parasitic elements and undesirable effects (self-heating (SH) and source-to-drain coupling through the substrate) whose impact on device performance increases enormously in downscaled devices. Specific features of UTBB FDSOI and MuGFET were analyzed.

We emphasized a crucial importance of wide-frequency DC-to-RF range characterization for fair device assessment and benchmarking. Relevant strength of this approach can be seen in some examples:

Proper extraction of SH effect parameters. SH effect in devices with various architectures and its impact on analog Figures of Merit (FoM) were analyzed [2-5]. Regardless thin-BOX (and thus expected SH reduction) in advanced MOSFETs, rather important channel temperature rise (~100°C) was revealed [2-5]. Much higher thermal resistance was revealed in short-channel UTBB MOSFETs comparing to their bulk counterparts [5] (Fig.1). Nevertheless, regardless stronger heating of UTBB FDSOI devices they outperform bulk counterparts in terms of analog FoM [5] (Fig. 1).

Parasitic coupling through the substrate was analyzed both in planar devices with thin BOX and in triple gate devices [1, 2, 4]. It was shown that BOX thinning in advanced devices results in enhanced source-to-drain coupling through the substrate, which in terms of parameters degradation can become even more important than widely-discussed SH effect (Fig. 2) [2]. However, introduction of so-called Ground Plane (GP) (i.e. highly-doped layer underneath the BOX) was shown to efficiently suppress coupling through the substrate [1, 2, 4] (Fig. 2). In the case of triple-gate devices, fin width engineering also allows suppression of this effect [1] (Fig.2).

Effect of extrinsic parasitic elements on advanced devices RF FoM. The developed procedure is based on extraction of complete small-signal equivalent circuit from S-parameter measurements at different bias conditions [1, 6]. We demonstrated that impact of parasitic elements becomes crucial with device downscaling and introduction of new 3D/thin-films architectures, dominating device performance [1]. Separate extraction of extrinsic and intrinsic parameters helps to optimize process and device configuration. Appropriate optimization allowed 28FDSOI MOSFETs to achieve f_T ~280 GHz, i.e. close to the ITRS requirements [4, 6].

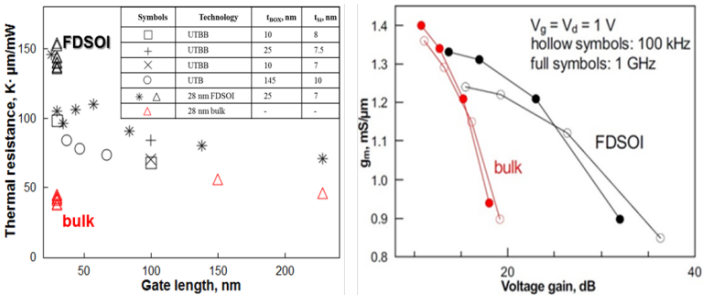

Figure 1: Thermal resistance in devices from various technologies (left). g_m vs. A_{vo} in bulk and FDSOI devices (right) [5].

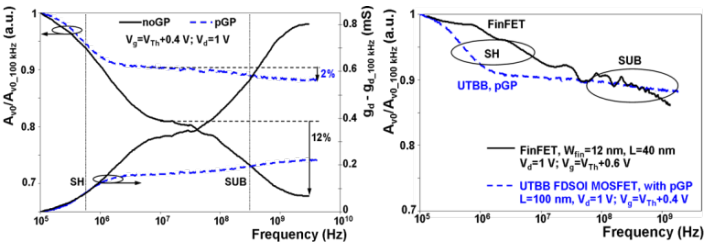

Figure 2: GP effect on g_d and A_{vo}. L=100 nm. W=30 μm. T_{box}=10 nm (left). A_{vo} vs frequency in UTBB MOSFETs and FinFETs [1] (right).

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