Lab on-chip for testing thin film materials: extraction of mechanical properties and coupled effects at the nanometer scale

Keywords : Thin films; Internal stress; Nanomechanical testing.

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Abstract – Thin films constitute the building blocks of a large number of modern technologies including protective coatings, microelectronic devices, bio-responsive membranes and photovoltaic cells. These nano-layers exhibit vastly different mechanical properties from their bulk counterpart. In this context, a lab-on-chip technique has been developed to extract the mechanical properties of thin films.

From a collaboration between Prof. Raskin (ICTEAM) and Prof. Pardoen (iMMC), a simple lab-on-chip concept has been created to assess the mechanical properties of submicron freestanding thin films [1]. It relies on the use of internal stresses generated in an "actuator layer" to apply a deformation to a "specimen layer" attached to it owing to the release of an underneath "sacrificial layer" (see Fig. 1). The simplest test structure configuration gives access to one point of the stress - strain curve of the specimen material while photolithography enables to reproduce this elementary tensile test structure thousands of times to generate the full stress - strain behaviour up to fracture.

This simple idea gives access to several extensions:

- The loading configuration can be changed by modifying the geometry of actuator and specimen beams;
- Relaxation tests can be performed by monitoring the displacement versus time of test structures;
- The deformation mechanisms can be observed by transmission electron microscopy. This requires an additional process step known as back-etching of the silicon substrate which consists in opening a cavity underneath the freestanding structures (see Fig. 2a);
- Electromechanical measurement can be performed by changing the specimen into a loop-shaped structure with isolated pads for electrical contacts. This enables to measure the piezoresistance of the specimen material (see Fig. 2b);
- The test structures can easily be stored under various environmental conditions (temperature, moisture, gas, irradiation, etc.) before release to determine the impact on properties or after release to see the impact on relaxation. The "authors" line at the top of the page is meant to mention all implied researchers, not only primary investigators. If possible, add a hyperlink for each

This lab-on-chip concept has already proven to be suitable for extraction of mechanical properties of ductile materials (Pd [2], AlSi, Ni, Cu, Pt, etc.) as well as brittle materials (monocrystalline Si, polycrystalline Si, oxides, nitrides, metallic glasses). The piezoresitance of silicon nanowires under high tensile stress has also been assessed through this technique [3].

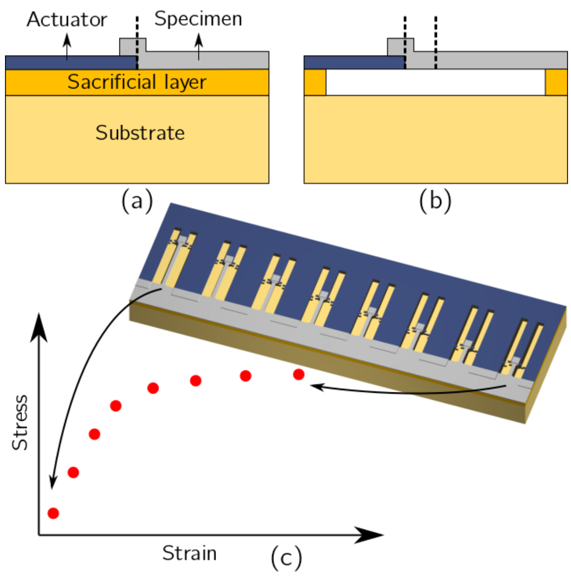

Figure 1: Principle of lab-on-chip concept: side view showing the different layers (a) before and (b) after etching of sacrificial layer, and (c) set of structures for extraction of full stress-strain curve.

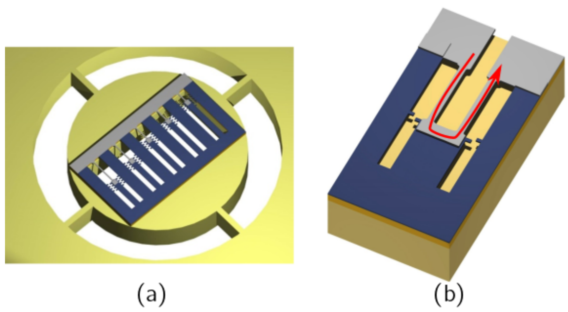

Figure 2: Designs of two extensions of the lab-on-chip concept : (a) Backetching for TEM analysis and (b) design of an elementary test structure for electro-mechanical characterization.

References

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