Trap-rich substrate enabling the RF Silicon-on-Insulator integration in all smartphones

Keywords : Silicon-on-insulator (SOI); RF; High frequency characterization; Substrate losses; Crosstalk; Non-linearity; Telecommunication device.

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Abstract* – *Silicon substrate losses and non-linearities were the limiting characteristics of Si-based MOSFET technologies to provide low-power and low-cost solutions to the mobile RF device market. Thanks to the trap-rich Silicon-on-Insulator (SOI) substrate invented at UCL and developed in collaboration with the French company SOITEC, RF SOI is becoming a mainstream technology which is implemented in all mobile devices today.

Silicon-based MOS technologies have been considered as a potential candidate for providing an efficient and cheap solution for RF mobile devices since the 1990's. The cutoff frequency of MOS transistors has been greatly increasing in the last decade due to the shrinking of the transistor channel size (the downscaling driven by the digital applications - Moore's law). However, substrate losses and crosstalk remained the killer feature of Si-based technologies for RF Front End Module (FEM) applications.

In 1997, Prof. J.-P. Raskin presented pioneering work on the RF performance of high-resistivity (HR) Silicon-on-Insulator (SOI) substrate material. The great potential of HR SOI substrate to reduce RF losses as well as the crosstalk in Si-based substrates was demonstrated [1]. Prior to this work, the scientific community considered the Si-based substrate as the limiting and blocking obstacle for working RF Front End Module ICs. In 2005, Prof. J.-P. Raskin's group presented the possibility of creating HR SOI substrates characterized with an effective resistivity as high as 10 kΩ.cm due to the silicon surface modification below the buried oxide (BOX) of a high resistivity SOI substrate [2]. The surface modification consists of the introduction of a high density of defects called traps at the BOX / HR-Si handle substrate. Those traps originate from the grain boundaries in a thin (300 nm-thick) polysilicon layer (Fig. 1). This high-resistivity characteristic, which is conserved after a full CMOS process, translates to very low RF insertion loss (< 0.1 dB/mm at 1 GHz) along coplanar waveguide (CPW) transmission lines and purely capacitive crosstalk similarly to quartz substrate [3]. It has been demonstrated that the presence of a trapping layer does not alter the DC or RF behavior of SOI MOS transistors [4]. Besides the insertion loss issue along interconnect lines, the generation of harmonics in the Si-based substrates has been investigated. We demonstrated that the harmonic level originating from the substrate is reduced (Fig. 2) by at least 20 dB by moving from standard resistivity SOI substrates ($\sim$ 10Ω.cm) to high resistivity SOI ($\sim$ 1 kΩ.cm), and more importantly, an additional drop of 40 dB is achieved with the innovative trap-rich HR SOI substrate [5]. This low harmonic level is comparable with insulating substrates. This discovery has led to two patents. Since 2009, Prof. Raskin's group has been collaborating with SOITEC (a company) to develop a lossless SOI substrate for RF applications. Due to the introduction of an engineered SOI substrate based on Prof. Raskin's discovery, SOITEC now provides a new type of HR-SOI called eSI™, for RF enhanced Signal Integrity substrate with a measured effective resistivity as high as 10 kΩ.cm. Thanks to the introduction of eSI, the RF SOI substrate can really be considered as a lossless Si-based substrate. Beyond the RF switch (Fig. 3), eSI RF-SOI technology opens the path for further system integration in the Front End Module space as well as even more complex mixed signal System-on-Chip (SoC).

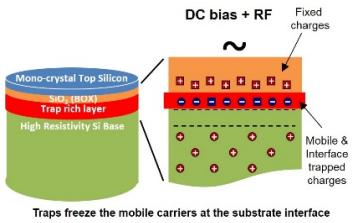

Figure 1: Cross-section of a trap-rich SOI substrate with its carrier distribution at equilibrium.

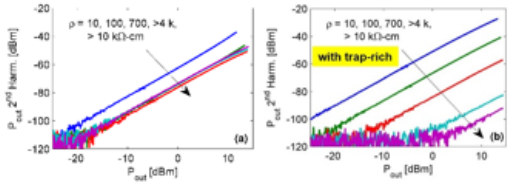

Figure 2: - Measured second harmonic output power of a 2,146-μm-long CPW line on n-type Si with different resistivities (a) without and (b) with a trap-rich polysilicon layer.

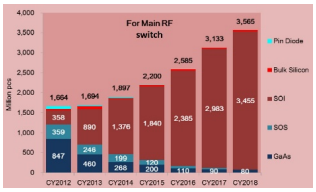

Figure 3: Rapid adoption of trap-rich SOI substrate for RF switches.

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